NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

CERTIFICATION PROGRAM IN SYNTHESIS & STATIC TIMING ANALYSIS

INFORMATION BROCHURE

National Institute of Electronics and Information Technology, NOIDA

Name of Institute: **Centre of Excellence in Chip Design** at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: Certification Program in Synthesis and Static timing Analysis

NIELIT: The National Institute of Electronics and Information Technology (NIELIT), is an autonomous scientific society under the administrative control of the Ministry of Electronics and Information Technology (MeitY), Government of India. NIELIT is actively engaged in Capacity Building and Skill Development in the areas of IECT. As of date, NIELIT has a Pan-India presence through a network of 51 own centers, more than 500 accredited centers, and 6500+ facilitation centres. NIELIT is also an active resource centre in conducting training programs in all technologies under the FutureSkills PRIME program especially stressing Cyber Security, Cyber Forensics, Blockchain, Artificial Intelligence, and IoT.

SoCTeamup: Founded at NSUT-IIF, SoCTeamup Semiconductors Pvt Ltd envisions redefining SoC design, aiming to create an IC design services platform that is at par with software design services, maximize the visibility of every skilled resource in the semiconductor realm, and democratize IC design process through the development of open-source and hybrid EDA design flows. Additionally, the company focuses on developing low-cost plug-and-play DFT/DFX solutions for next-generation SoCs and mission-critical systems. SoCTeamup aspires to create a digital platform that redefines the landscape of ultra-low-cost SoC design and manufacturing services**.**

Course Objective: Certification Program in Synthesis and Static timing provide a comprehensive overview of:

- Very Large-Scale Integration concepts, covering digital design methodologies, ASIC technologies, physical design and static timing analysis
- Synthesis and Static timing Analysis performed using **Genus & Tempus EDA tools of Cadence**.
- Participants will gain hands-on experience with **Cadence EDA tool suite** explore power-efficient design strategies and delve into emerging trends.
- The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Sh. Pankaj Shukla Additional Director/Scientist E & OIC CoE in Chip Design, NIELIT Noida

PRASHANT PAL (Scientist-C)

National Institute of Electronics and Information Technology, NOIDA

Duration: 60 Working days @ 3 Hrs per day per session (180 Hours)

NOTE: Classroom Based Instructor Led Training. Limited seats (Only 20)

Eligibility:

1. Students who have completed or pursuing B.Tech/ M.Tech/M.Sc. in, Electronics & Communication Engineering, Electrical Engineering, Computer Science or relevant fields
2. Recent graduates/Faculty members seeking to enter the semiconductor industry
3. Research Scholars, Faculty members, and Industry professionals can also enroll

Prerequisites: -

1. Digital Electronics knowledge (logic gates, circuits, state machines).
2. Calculus (differentiation, integration) for timing analysis.
3. Strong problem-solving and analytical skills are essential.

Course Fees: Rs. 25,488/- (incl. GST)

Tentative Course Date: Please refer registration link.

Registration Process: Candidates have to apply in the prescribed application form through https://regn.nielitvte.edu.in/in_campus_courses.php. The duly filled form along with the course fees receipt has to be submitted in online mode through the above link. The Fees deposited are Non-Refundable.

Course Outcomes: Upon completion of the Certification Program in Synthesis and Static timing Analysis students will be well-prepared for lucrative opportunities in the Indian and international job markets. By completing this course, students will also be able to:

- **Appreciate** the fundamental concepts of RTL2GDS VLSI design flow
- **Design** digital circuits using Hardware Description Languages (HDLs) like Verilog or VHDL, considering synthesis constraints.
- **Utilize** logic synthesis tools to translate HDL code into optimized gate-level netlists.
- **Perform** basic physical design tasks, including floor planning, clock tree synthesis, placement ,power planning, routing and constraint management, for GDS generation.

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- Constraining the design with SDC command constraining the design with SDC commands.
- Timing Analysis of Different Paths
- Analyze reports to identify timing problems
- Perform timing debug with ECO
- Practical STA Issues and Solutions

Key Highlights:

- All Classes in physical mode with one- to-one mentorship
- Use of Licensed **EDA tool of Cadence**
- Real-time industry project exposure
- Course Designed by industry experts with cumulative experience of 40+ years in leading semiconductor companies and executed 30+ Tapeouts

- **This course will help the candidate crack job interviews in semiconductor industries working with the Cadence EDA tool.**

Topics to be Covered

- **Introduction to VLSI design concepts, applications, and design flows**
- **HDLs using Verilog**

- **Synthesis-synthesis flow, optimization techniques, exemption and constraints Constraining design for timing area and power, report generation, analysis and debug the result**

- **Physical Design-floor planning, clock tree synthesis, placement, power planning, routing**

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- **Static Timing analysis-containing design with SDC commands, Timing analysis of different paths, analysis timing report, Practical STA issues and solution**
- **Fixing timing violation using ECO**
- **Hands on Project using Cadence tool suite.**

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode.
For any queries and more details please contact on **8218724641/9711177638**

Course Venue

Centre of Excellence in Chip Design, NIELIT NOIDA Centre, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:
https://regn.nielitvte.edu.in/in_campus_courses.php
or
Through Android App "**NIELIT Kaushal Setu**"

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