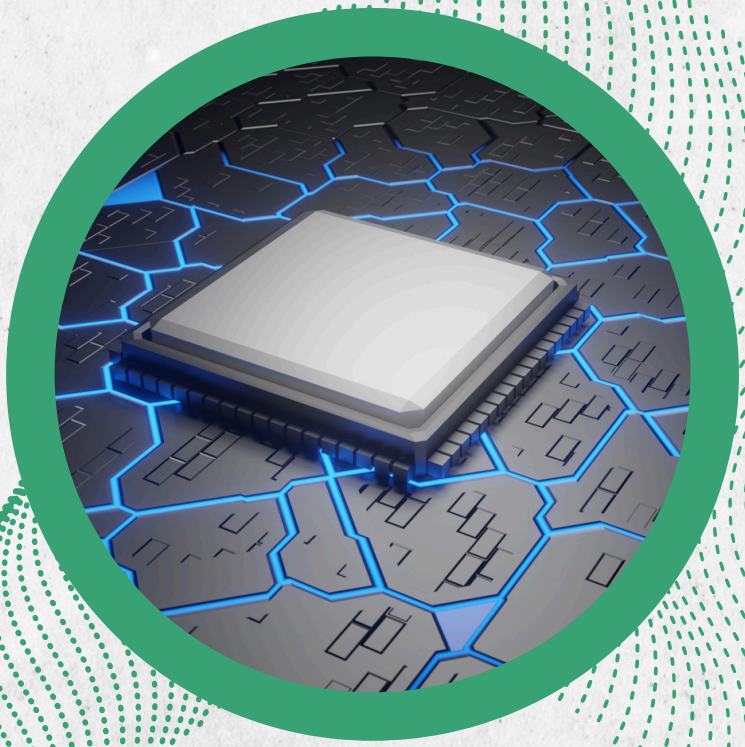
NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

TWO-WEEK FACULTY DEVELOPMENT TRAINING PROGRAM ON VLSI DESIGN

INFORMATION BROCHURE



NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY, NOIDA

Name of Group: Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: Two-week Faculty Development and Training Program on VLSI Design

Objective: The two-weeks VLSI course aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with **Cadence EDA toolsuite**, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Duration: 10 Days (60 Hours) (6hrs/day)

NOTE: Only in physical mode. **Limited seats (Only 20)**

Eligibility: Faculty members teaching B.Tech/M.Tech/B.Sc/M.Sc/Diploma courses

Note: Research Scholars, Faculty members and Industry professionals can also enrol

Prerequisites: -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

Course Fees: Rs. 3000/- (incl. GST)

Course Date: 01st July 2024 (Tentative)

Registration Process: Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/in_campus_courses.php or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

Topics to be covered:

Day 1	**Custom Design Flow**	• FPGAs: Types, Architecture, Applications
Day 2		**FPGAs: Hands on Session** • HDL Design, Simulation • Dumping Code into FPGA • Hardware Debugging • Mark Debug Feature • Integrated Logic Analyzer (ILA) core

Partha P. Adhikari,
Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

PRASHANT PAL
(Scientist-C)

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Day 3		• CMOS Analog/Digital Circuit Design Using Cadence Virtuoso • Schematic Editor • Symbol Creation Using Cadence Virtuoso Symbol Editor Transistor Level Layouts Creation Using Cadence Virtuoso Layout Editor
Day 4	**ASIC Design Flow**	• Wire parasitics and their impact on circuit performance • Modeling and simulation of on-chip wires Timing analysis
Day 5		**Linux and VI Editor** • RTL Design Using HDL • Introduction to Verilog syntax and constructs • Designing combinational and sequential logic using HDL
Day 6		• Basic Cadence Genus Synthesis Flow -Input required for synthesis, synthesis stages, optimization techniques for best area ,power and timing
Day 7		• Hands on training on-Introduction to synthesis tools and libraries , Synthesizing RTL designs for target technologies , Optimizing design for best area, power, and performance
Day 8		• Digital implementation using Cadence Innovus • Introduction to floorplanning, placement, power planning, routing
Day 9		• Hands on floorplanning ,placement, power planning using Innovus • Defining the size of the chip, arranging, and positioning hard macros, IO pads and other desired objects and defining a power grid for the design
Day 10		• Timing Analysis and Debug using Cadence Tempus • Q&A session and Quiz

* There will be 6 Hours Session per day
* Cadence tools will be used for hands on training
* For Layout editor-Virtuoso, Synthesis Flow -Genus, Digital implementation Flow –Innovus, Timing analysis & Debug-Tempus

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode.
For any queries and more details please contact on **8218724641/9711177638**

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Course Venue

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:

https://regn.nielitvte.edu.in/in_campus_courses.php

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