इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

रा.इ.सू.प्रौ.सं NIELIT

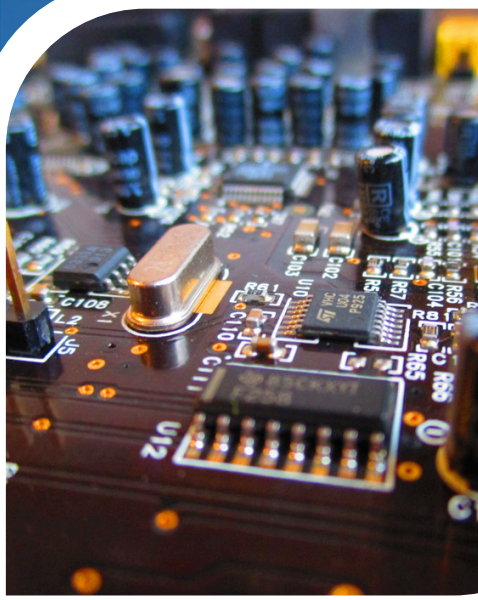
SoCTeamup

ADVANCE CERTIFICATION PROGRAM IN VLSI DESIGN

Part I - Certification Program in RTL to GDS-II and Physical Design
Part II -Advance Certification Program in VLSI Design and DFT

INFORMATION BROCHURE

NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY, NOIDA



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NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY (NIELIT),

(Centre of Excellence in Chip Designing, Noida Centre)
(An Autonomous Scientific Society of Ministry of Electronics & IT, (MeitY), Govt. of India)

Name of Institution: Centre of Excellence in Chip Designing at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: Advance Certification Program in VLSI Design

NIELIT: The National Institute of Electronics and Information Technology (NIELIT), is an autonomous scientific society under the administrative control of the Ministry of Electronics and Information Technology (MeitY), Government of India. NIELIT is actively engaged in Capacity Building and Skill Development in the areas of IECT. As of date, NIELIT has a Pan-India presence through a network of 51 own centers, more than 500 accredited centers, and 6500+ facilitation centres. NIELIT is also an active resource centre in conducting training programs in all technologies under the FutureSkills PRIME program especially stressing the Cyber Security, Cyber Forensics, Blockchain, Artificial Intelligence, and IoT.

SoCTeamup: Founded at NSUT-IIF, SoCTeamup Semiconductors Pvt Ltd envisions to redefine SoC design, aiming to create an IC design services platform which is at par with software design services, maximize visibility of every skilled resource in the semiconductor realm, and democratize IC design process through development of open-source and hybrid EDA design flows. Additionally, the company focuses on developing low-cost plug-and-play DFT/DFX solutions for next generation SoCs and mission critical systems. SoCTeamup aspires to create a digital platform that redefines the landscape of ultra-low-cost SoC design and manufacturing services.

PARTHA P. ADHIKARI
Additional Director/Scientist 'E' & OIC, CoE Chip Design Noida Centre

PRASHANT PAL
(Scientist - C)

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Course Objective: The course aims to provide a comprehensive overview of:

- Very Large-Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing.
- RTL to GDSII, Semi-Custom & Full-Custom Design Flows using **Virtuoso, Genus, Innovus, Tempus EDA tools of Cadence.**
- Participants will gain hands-on experience with **Cadence EDA** tool suite, explore power-efficient design strategies, and delve into emerging trends.
- The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP Semiconductors to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Current Job Scenario in VLSI Design: The job scenario in the VLSI Design industry in India and abroad is characterized by robust growth and high demand for skilled professionals. In India, the VLSI Design sector has experienced significant expansion, fueled by the country's emergence as a global hub for semiconductor manufacturing and research. With the rise of initiatives such as the "Make in India" campaign and the National Policy on Electronics, the Indian government has prioritized the development of VLSI Design industry, offering incentives and infrastructure support to attract investments and foster innovation. This has led to the establishment of numerous semiconductor fabrication units and design centers across the country, creating a plethora of job opportunities for VLSI engineers. Similarly, abroad, countries like the United States, China, and Taiwan continue to drive innovation and investment in VLSI Design, offering lucrative career prospects for skilled professionals. Overall, the VLSI Design industry presents a dynamic and promising landscape for individuals seeking rewarding careers both in India and on the international stage.

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Duration for Part-I : 40 Working days @ 6 Hrs per day per session (240 Hours)/2 Months
Duration for Part-II : 40 Working days @ 6 Hrs per day per session (240 Hours)/2 Months

NOTE: Only in physical mode. **Limited seats (Only 20)**

Eligibility: Students who have completed or pursuing B.Tech/ M.Tech/ M.Sc. in Electronics/Computer/Electrical or relevant discipline

Note: Research Scholars, Faculty members and Industry professionals can also enroll

Prerequisites: -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

Course Fees for Part -I: Rs. 33,984/- (incl. GST)
Course Fees for Part -II: Rs. 33,984/- (incl. GST)

Note: Course fees can be paid in two equal instalments

Course Date for Part-I : Tentatively starting from 03 June 2024*
Course Date for Part-II: Tentatively starting from 05 Aug 2024*

Registration Process: Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/ or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees has to be submitted in online mode through the above link.
Note: The Fees deposited is Non-Refundable

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Course Outcomes: Upon completion of the Advanced Certification Program in VLSI Design, students will be well-prepared for lucrative opportunities in the Indian and international job markets, equipped with:

- Proficiency in using industry-standard EDA tools, ensuring they can efficiently navigate complex design tasks and contribute effectively to project teams.
- Expertise in emerging trends such as System-on-Chip (SoC) design and low-power optimization, enhancing their competitiveness and adaptability in diverse work environments.

Salient Features:

- All Classes in physical mode with one-to-one mentorship
- Use of Licensed EDA tool of **Cadence** which includes **Spectre, Virtuoso, Genus, Innovus, Modus, Quantus, Tempus & Xcelium**
- Real-time industry project exposure
- Placement assistance

Course Content:

Module #	Module Description	Contents with Hands on
Module 1 (Part -I)	RTL-GDSII flow	• Introduction to RTL design and its role in the chip design process • RTL coding practices and guidelines • Logic synthesis and technology mapping • Physical design considerations at RTL • Design constraints and timing analysis • Hands-on exercises using industry-standard RTL tools

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Module 2 (Part -I)	Design Verification	• Introduction to verification methodologies, including simulation and functional verification. • Writing testbenches and test vectors • Concept of OOPs in System Verilog • IPC in System Verilog • Code coverage and functional coverage analysis • Assertion based Verification • UVM (Universal Verification Methodology) for advanced verification • UVM based classes • TLM • Config_db and resource_db in UVM • Practical verification project assignments
Module 3 (Part -II)	DFT	• Introduction to DFT principles and goals • Scan chains and scan design techniques • Built-in self-test (BIST) methodologies • Boundary scan (JTAG) and test access mechanisms • Test pattern generation and fault coverage analysis • Practical DFT design projects with real-world applications
Module 4 (Part -II)	Project based on Industry standard ASIC Implementation	

- There will be 6 Hours Session per day.
- Placement assistance will only be provided to the students who have both Part-I and Part-II of the course

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Mode of Payment:
Fees can be paid either by debit/credit card or in any online mode.

For any queries and more details please contact on **8218724641/9711177638**

Course Venue

Centre of Excellence in Chip Designing, NOIDA Centre NIELIT, PS-1D, Behind Brahmaputra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301, Walking distance from **Botanical Garden Metro station**

Office Address
CoE in Chip Designing, Noida, PS-1D, Behind Brahmaputra Shopping Complex, Sector 29, Arun Vihar, Noida, Uttar Pradesh 201303, Walking distance from **Botanical Garden Metro station**

Registration Link:
QR code for registration link:
https://regn.nielitvte.edu.in/in_campus_courses.php
or
Through Android App "**NIELIT Kaushal Setu**"

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