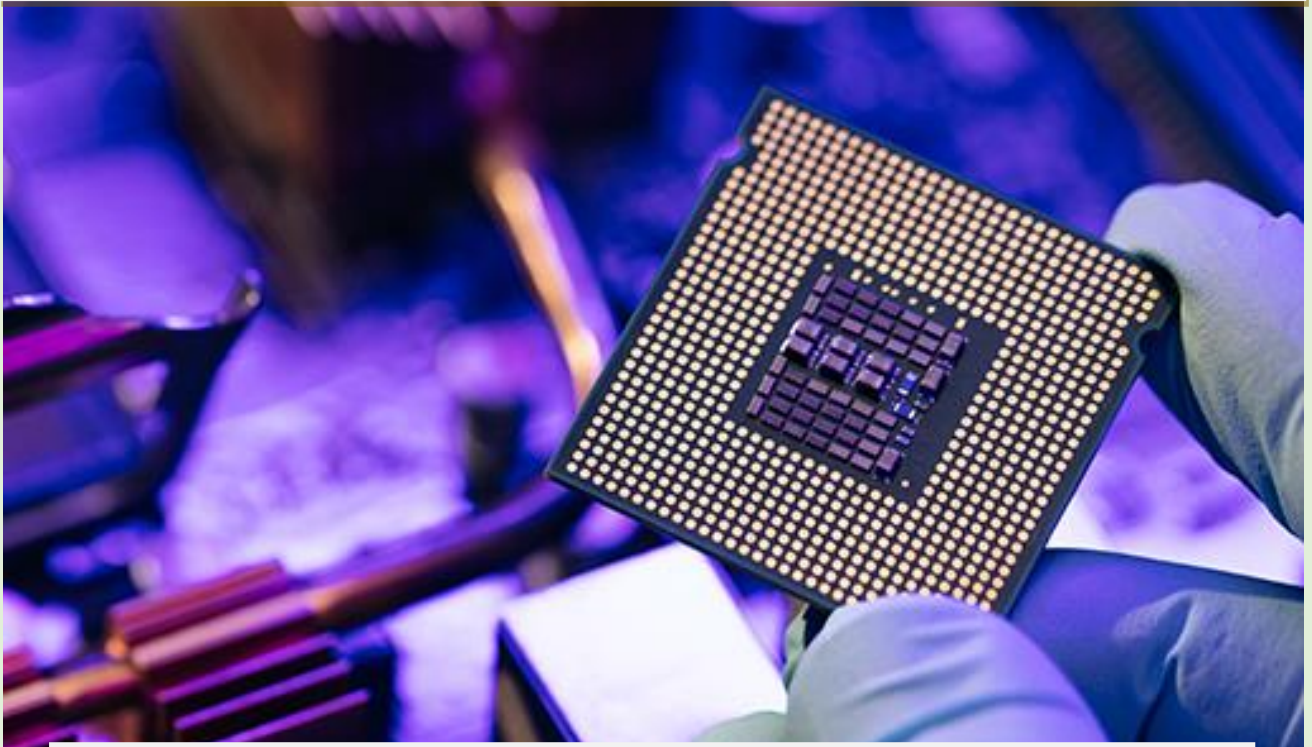




**NATIONAL INSTITUTE OF
ELECTRONICS & INFORMATION
TECHNOLOGY NOIDA**

**CERTIFICATION/INTERNSHIP
PROGRAMME IN ASIC DESIGN**



**INFORMATION
BROCHURE**

Name of Institute: Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: Certification/Internship Programme in ASIC Design

NIELIT: The National Institute of Electronics and Information Technology (NIELIT), is an autonomous scientific society under the administrative control of the Ministry of Electronics and Information Technology (MeitY), Government of India. NIELIT is actively engaged in Capacity Building and Skill Development in the areas of IECT. As of date, NIELIT has a Pan-India presence through a network of 51 own centers, more than 500 accredited centers, and 6500+ facilitation centres. NIELIT is also an active resource centre in conducting training programs in all technologies under the FutureSkills PRIME program especially stressing the Cyber Security, Cyber Forensics, Blockchain, Artificial Intelligence, and IoT.

SoCTeamup: Founded at NSUT-IIF, SoCTeamup Semiconductors Pvt Ltd envisions redefining SoC design, aiming to create an IC design services platform that is at par with software design services, maximize the visibility of every skilled resource in the semiconductor realm, and democratize IC design process through the development of open-source and hybrid EDA design flows. Additionally, the company focuses on developing low-cost plug-and-play DFT/DFX solutions for next-generation SoCs and mission-critical systems. SoCTeamup aspires to create a digital platform that redefines the landscape of ultra-low-cost SoC design and manufacturing services.

Course Objective: The Internship Program in ASIC Design course aims to provide a comprehensive overview of:

- Very Large-Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing.
- RTL to GDSII, Semi-Custom & Full-Custom Design Flows using **Virtuoso, Genus, Innovus, Tempus EDA tools of Cadence**.
- Participants will gain hands-on experience with **Cadence EDA tool suite** explore power-efficient design strategies, and delve into emerging trends.
- The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Current Job Scenario in VLSI Design: According to Deloitte, the workforce for the semiconductor industry will need to increase by more than 1 million skilled people by 2030. Over 1 lakh engineering and smart manufacturing graduates will be required for this industry. India can command thousands of these jobs as the industry starts to grow. With the rise of initiatives such as the "Make in India" campaign and the National Policy

Partha P. Adhikari,

Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

PRASHANT PAL

(Scientist-C)

on Electronics, the Indian government has prioritized the development of the VLSI Design industry, offering incentives and infrastructure support to attract investments and foster innovation. This has led to the establishment of numerous semiconductor fabrication units and design centers across the country, creating a plethora of job opportunities for VLSI engineers. Similarly, abroad, countries like the United States, China, and Taiwan continue to drive innovation and investment in VLSI Design, offering lucrative career prospects for skilled professionals. Overall, the VLSI Design industry presents a dynamic and promising landscape for individuals seeking rewarding careers both in India and on the international stage.

Duration: 40 Working days @ 3 Hrs per day per session (120 Hours)

NOTE: Classroom Based Instructor Led Training. Limited seats (Only 20)

Eligibility:

1. Students who have completed or pursuing B.Tech/ M.Tech/M.Sc. in, Electronics & Communication Engineering, Electrical Engineering, Computer Science or relevant fields
2. Recent graduates/Faculty members seeking to enter the semiconductor industry
3. Research Scholars, Faculty members, and Industry professionals can also enroll

Prerequisites: -

1. Electrical Engineering/Electronics basics (circuits, voltage, current).
2. Digital Electronics knowledge (logic gates, circuits, state machines).
3. Calculus (differentiation, integration) for timing analysis.
4. Basic C/C++ or scripting (optional, for HDLs and automation).
5. Strong problem-solving and analytical skills are essential.

Course Fees: Rs. 16,992/-/- (incl. GST)

Attractive Discount for Group of 5 Students or more from the same College/Institution/University

Tentative Course Date: Starting from 27 May 2024

Registration Process: Candidates have to apply in the prescribed application form through https://regn.nielitvte.edu.in/in_campus_courses.php. The duly filled form along with the course fees receipt has to be submitted in online mode through the above link. The Fees deposited are Non-Refundable.

Course Outcomes: Upon completion of the Internship Program in ASIC Design, students will be well-prepared for lucrative opportunities in the Indian and international job markets. By completing this course, students will also be able to:

- **Appreciate** the fundamental concepts of VLSI design and differentiate between major design flows (RTL to FPGA, RTL to GDS, Full-Custom).
- **Analyze** the impact of CMOS fabrication processes on different design flows.

Partha P. Adhikari,

Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

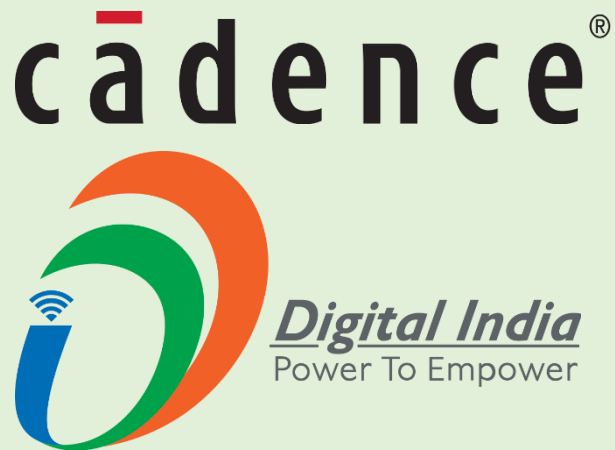
PRASHANT PAL

(Scientist-C)

- **Design** digital circuits using Hardware Description Languages (HDLs) like Verilog or VHDL, considering synthesis constraints.
- **Utilize** logic synthesis tools to translate HDL code into optimized gate-level netlists.
- **Implement** digital circuits on FPGAs, understanding the FPGA architecture and design flow (synthesis, PnR, bitstream generation).
- **Apply** design for manufacturability (DFM) techniques when targeting an ASIC design flow (RTL to GDS-II).
- **Perform** basic physical design tasks, including floor planning and constraint management, for GDS generation.
- **Comprehend** the basic principles of full-custom design flow (schematic capture, layout, verification).

Key Highlights:

- All Classes in physical mode with one-to-one mentorship
- Use of Licensed **EDA tool of Cadence**
- Real-time industry project exposure
- Course Designed by industry experts with cumulative experience of 40+ years in leading semiconductor companies and executed 30+ Tapeouts
- **This course will help the candidate crack job interviews in semiconductor industries working with the Cadence EDA tool.**



Topics to be Covered

- Introduction to VLSI design concepts, applications, and design flows
- HDLs using Verilog
- Synthesis
- RTL to GDS Flow
- Physical Design & Static Timing analysis
- Advanced Topics & GDS Generation
- Industry-relevant Project

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode.

For any queries and more details please contact on **8218724641/9711177638**

Partha P. Adhikari,

Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

PRASHANT PAL

(Scientist-C)

Course Venue

Centre of Excellence in Chip Design, NIELIT NOIDA Centre, PS-1D, Behind Brahampurtra
Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:

https://regn.nielitvte.edu.in/in_campus_courses.php

or

Through Android App "[NIELIT Kaushal Setu](#)"



Partha P. Adhikari,

Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

PRASHANT PAL

(Scientist-C)