NCVET Code

2022/EHW/NIELIT/05319

NSQF QUALIFICATION FILE
Approved in 16th NSQC meeting – NCVET- Dated: 24th February, 2022

QUALIFICATION FILE - CONTACT DETAILS OF THE SUBMITTING BODY
Name and address of submitting body:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY

NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8,

Dwarka, New Delhi-110077

Name and contact details of individual dealing with the submission

Name	**:**	Ankit Kumar
Position in the organization	**:**	Scientist-'B'
Address if different from above	**:**	NA
Tel number(s)	**:**	09074841785
E-mail address	**:**	ankit@nielit.gov.in

List of documents submitted in support of the Qualifications File

Annexure 1: Detailed Syllabus and lesson plan of the course
Annexure 2: Evidence of Course requirement in the industry
Annexure 3: Evidence of Job requirement from the industry
Annexure 4: Evidence of validation from industries

Model Curriculum to be added which will include the following:

- Indicative list of tools/equipment to conduct the training

Attached in Annexure 5

- Trainers qualification

Attached in Annexure 6

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SUMMARY

1	**Qualification Title**	Foundation course in VLSI Design
2	**Qualification Code, if any**	Will be given by NCVET post-approval Sector: Electronics
3	**NCO code and occupation**	2152.9900 (Electronics Engineers, Other)
4	**Nature and purpose of the qualification (Please specify whether qualification is short term or long term)**	**Nature:** ❖ This certificate course will help in employment. ❖ This Qualification is aligned to Level 4 **Purpose:** ❖ To train the students to be ready for VLSI Design and RTL Design, FPGA Engineer Job. ❖ To upgrade the skills of people already in work in RTL coding or Chip designing other allied areas of this technology ❖ Entrepreneurship development
5	**Body/bodies which will award the qualification**	National Institute of Electronics and Information Technology NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
6	**Body which will accredit providers to offer courses leading to the qualification**	NIELIT
7	**Whether accreditation/affiliation norms are already in place or not, if applicable (if yes, attach a copy)**	The Handbook for TP accreditation norm is available at: https://www.nielit.gov.in/content/nsqf
8	**Occupation(s) to which the qualification gives access**	VLSI Design Engineer VLSI Test Engineer RTL Design Engineer
9		. ❖ **VLSI Design Engineer:** Design and development of VLSI based design, IP Core development.

	Job description of the occupation	❖ **VLSI Test Engineer**: verification, test patterns generation ❖ **RTL Design Engineer**: Develop design specifications based on the project requirements.
10	**Licensing requirements**	NA
11	**Statutory and Regulatory requirement of the relevant sector (documentary evidence to be provided)**	NA
12	**Level of the qualification in the NSQF**	Level 4
13	**Anticipated volume of training/learning required to complete the qualification**	90 Hours
14	**Indicative list of training tools required to deliver this qualification**	Attached in Annexure 5
15	**Entry requirements and/or recommendations and minimum age**	Final Year Polytechnic Diploma in Electronics /Electrical/ Instrumentation **or** 3rd semester B.E/B.Tech in Electronics/Electronics & Communication/ Electrical/ Electrical & Electronics/Instrumentation
16	**Progression from the qualification (Please show Professional and academic progression)**	Professional: RTL Engineer > Sr. RTL Engineer Test Engineer > Design Engineer Academic: i) Horizontal Progression: Courses in the area of Digital VLSI, FPGA and Layout Design ii)Vertical Progression Advance Diploma in VLSI physical Design Engineer,PG Diploma in VLSI and Embedded hardware Design, M.Tech in VLSI

17	**Arrangements for the Recognition of Prior learning (RPL)**	Candidates with 1 year of experience in the relevant field may apply directly for evaluation.
18	**International comparability Where known (research evidence to be provided)**	NA
19	**Date of planned review of the Qualification.**	After Every 5 years
20	**Formal structure of qualification**	

Module Code	Module Name	Mandatory/ Optional	Estimated Size (Learning Hours)	Level
1	Introduction to Digital Electronics	Mandatory	10	4
2	Basics of Digital VLSI Technology	Mandatory	12	4
3	Fabrication Process and Layout Design Rules	Mandatory	6	4
4	Digital CMOS Design	Mandatory	12	4
5	Hardware Modeling Using Verilog	Mandatory	28	4
6	Implementation of Logic gates/circuits in Verilog using Tool (ModelSim or Xilinx)	Mandatory	22	4

SECTION 1

ASSESSMENT

21	**Body/Bodies which will carry out assessment:** The Examination Wing National Institute of Electronics and Information Technology NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
22	**How will RPL assessment be managed and who will carry it out?** RPL assessment will be done by Examination Wing, NIELIT. Candidates can register as direct candidate with NIELIT and apply for evaluation.
23	**Describe the overall assessment strategy and specific arrangements**

	which have been put in place to ensure that assessment is always valid, reliable and fair and show that these are in line with the requirements of the NSQF. The emphasis is on practical demonstration of skills & knowledge based on the performance criteria. Student is required to pass in all OUTCOMEs individually and marks are allotted. The Following assessment methodologies are used. 1. Written Assessment (Multiple Choice Questions) 2. Practical Assessment & Assignments 3. Project The assessment results are backed by following evidences. 4. The theory assessment is carried in online remote proctored mode. 5. Proctors authenticate the candidate based on registration details, pre-test image captures and I-card in possession of the candidate. 6. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds. 7. Practical examination/Internal Assessment/ Project/Presentation/Assignment would be evaluated internally.

24. ASSESSMENT EVIDENCE

Title of Unit/Component:

Outcomes to be assessed	Assessment Criteria for the outcome	Means of Assessment		
		Total Marks	Written	Practical
Fundamentals of Digital VLSI	Fundamentals of Digital Electronics	20	20	0

	Digital VLSI Technology	20	10	10
	Total	**40**	**30**	**10**
Digital CMOS Technology and Layout design	Digital CMOS Technology	20	20	0
	Layout design and Digital CMOS Design	30	10	20
	Total	**50**	**30**	**20**
Hardware Modeling Using Verilog	Verilog Programming	30	20	1 0
	Implementation of Logic gates/circuits in Verilog using Tool (ModelSim or Xilinx)	40	20	20
	Total	**70**	**40**	**30**
Internal Assessment		**20**	**0**	**20**
Assignment		**20**	**0**	**20**
Total Marks		**200**	**100**	**100**

Means of assessment

S. No	Examination Pattern	Modules Covered	Duration in Minutes	Maximum Marks
1	Theory	1-6	90	100
3	Practical	1-6	180	60
4	Internal Assessment	1-6	-	20
5	Assignment	1-6	-	20
Total				**200**

Note:

1. Pass percentage would be 50% marks in each component, with aggregate pass percentage of 50% and above.
2. Grading will be as under:

Grade	S	A	B	C	D
Marks Range (in %)	>=85%	>=75% and <85%	>=65% and <75%	>=55% and <65%	>=50% and <55%

3. Theory examination would be conducted online and the paper comprise of MCQ and each question will carry 1 mark.
4. Practical examination/Internal Assessment/Assignment would be evaluated internally.
5. Candidate may apply for re-examination within the validity of registration.
6. The examinations would be conducted in English Language only.

SECTION 2

25. EVIDENCE OF LEVEL

Title: Foundation course in VLSI Design			**Level : 4**
NSQF Domain	**Outcomes of the Qualification/Component**	**How the job role relates to the NSQF Level Descriptors**	**NSQF Level**
Process required	The candidate is required to apply the Advanced digital design concepts, Verilog HDL coding skills and FPGA based prototyping skills for translation of specification to RTL Design and FPGA prototyping	Job that requires well developed skill, with clear choice of procedures in familiar context.	4
Professional knowledge	Factual knowledge about: - Terminologies associated with Digital design, HDL & FPGA prototyping. Elements Melay & More FSMs, ASMs, data path control path, lexical conventions, mega plug in wizards, processor cores etc.	Knowledge of facts, principles, processes and general concepts, in a field of work or study.	4
Professional skill	Selection of Appropriate Development board and tools available now a days for Embedded Hardware and Software	Candidate will have a wide range of specialized technical skill, clarity of	4

	implementation	knowledge and practice in broad range of activity involving standard and non-standard practices.	
Core skill	Language to communicate with written or oral, with required clarity, skill to basic arithmetic and algebraic principles, basic understanding of social, political and natural environment	Desired mathematical skill; understanding of social, political; and some skill of collecting and organizing information, communication.	4
Responsibility	Candidate will be able to work independently in front end VLSI with responsibility required and he can guide the works of his team members	Responsibility for own work and learning and some responsibility to other's works and learning.	4

NSQF QUALIFICATION FILE

SECTION 3

EVIDENCE OF NEED

26	**What evidence is there that the qualification is needed?** Attached in Annexure 2
27	**What is the estimated uptake of this qualification and what is the basis of this estimate?** Estimated uptake is 30 students per Batch with 4 Batches per Year and on the basis of Facilities and Infrastructure in respective NIELIT Centre.
28	**What steps were taken to ensure that the qualification(s) does (do) not duplicate already existing or planned qualifications in the NSQF? Give justification for presenting a duplicate qualification** The qualification is originally designed by curriculum head, industrial expert, and academic professional experts. The work group under the guidance of curriculum development committee already conducted desk search as well as refers the qualification packs for as a supporting document for the mapping of curriculum. As per the search it is found that, there are Qualification on NQR portal in VLSI, however essential qualification and purpose of the qualification is different from any other qualification.
29	**What arrangements are in place to monitor and review the qualification(s)? What data will be used and at what point will the qualification(s) be revised or updated? Specify the review process here** Based on feedback by participants, employers and based on market survey the qualification will be reviewed in every 5 years.

SECTION 4

EVIDENCE OF PROGRESSION

30	**What steps have been taken in the design of this or other qualifications to ensure that there is a clear path to other qualifications in this sector?** This qualification has been designed in consultation with industry and domain expert keeping in mind today's need. Qualification file is finalized after discussion and modification through internal committees of NIELIT. Evaluation criteria have been added to ensure progression to related path ways identified as per career path.