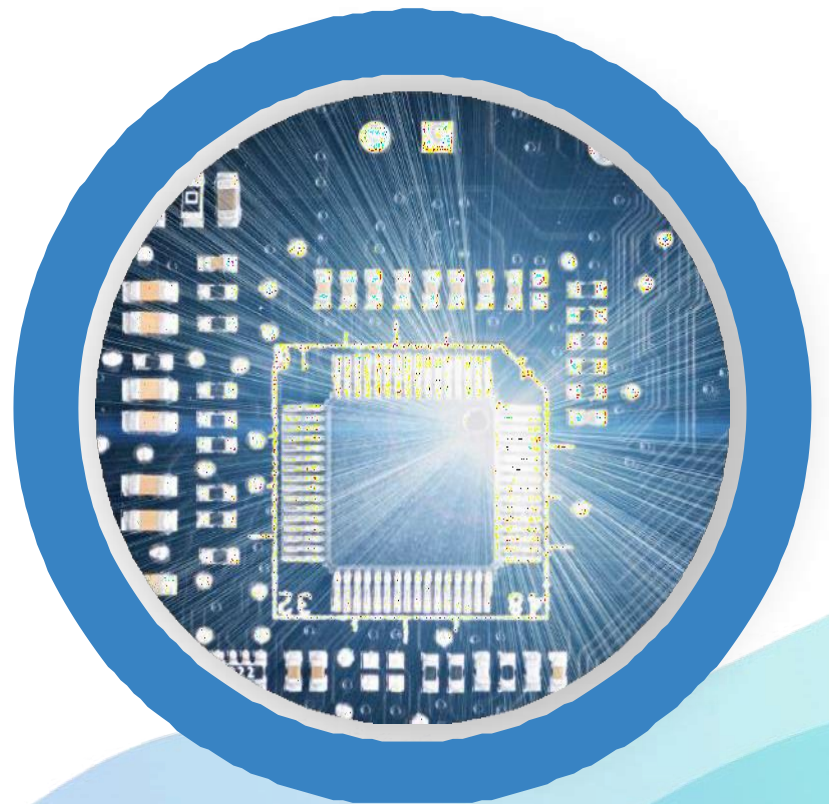


NATIONAL INSTITUTE OF ELECTRONICS &
INFORMATION TECHNOLOGY NOIDA

VLSI Design Flow (Online Mode)

INFORMATION BROCHURE



**NATIONAL INSTITUTE OF ELECTRONICS AND
INFORMATION TECHNOLOGY, NOIDA**

Name of Group: Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoC Teamup Semiconductors Pvt Ltd as industry partner

Name of Course: VLSI Design Flow (Online Mode)

Objective: The Training in Program on VLSI Design flow (Online Mode) aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, RTL ,synthesis , physical design. Participants will gain hands-on experience with open source **EDA tool** , explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Duration: 08 Days (42 hours)

Mode of Delivery: Online mode

Eligibility: Staff in Polytechnic, ITI, and PGT (Post-Graduate STEM Teachers) in schools.

Note: Research Scholars, Faculty members and **Industry professionals** can also enroll

Prerequisites: -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a Unix/Linux environment and command-line interface

Course Fees: Free for Faculty

Registration Process: Candidates have to apply in prescribed application form through online registration portal [https:// https://coenoida.in /](https://coenoida.in/).

Topics to be Covered

- Overview of VLSI Design Flow
- Basics of digital electronics
- Linux basics for VLSI design
- Hardware Modeling: Introduction to Verilog
- RTL Synthesis
- Basic Concepts for Physical Design
- Floorplanning, clock tree synthesis, routing

Pankaj Shukla ,
Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

PRASHANT PAL
(Scientist-C)

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Day	Session 1	Session 2
Day 1	Introduction to VLSI Design & Digital Electronics	Fundamentals of Digital Electronics (Logic Gates)
Day 2	Combinational and sequential circuits	Hands-on: Simulating Logic Gates using Logisim/Deed simulator
Day 3	Linux Basics for VLSI Design	Hands-on: Linux Commands and VI Editor
Day 4	Introduction to Verilog Programming	Hands-on: Verilog for Combinational Circuits
Day 5	Verilog Programming	Hands-on: Simulation of Sequential Circuits in Verilog
Day 6	Introduction to Synthesis	Hands-on: Synthesis with Yosys
Day 7	Introduction to Physical Design	Hands-on: Physical Design Tools (OpenROAD/Q flow)
Day 8	Review and Q&A	Online Feedback, Evaluation & Conclusion Session

* There will be 5.5 Hours Session per day in **online mode**.

Mode of Payment: Free for Faculty

For any queries and more details please contact on

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PRASHANT PAL
(Scientist-C)

**NATIONAL INSTITUTE OF ELECTRONICS AND
INFORMATION TECHNOLOGY, NOIDA**

Course Venue: Online

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping
Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:

<https://coenoida.in>

or

Through Android App “[NIELIT Kaushal Setu](#)”



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