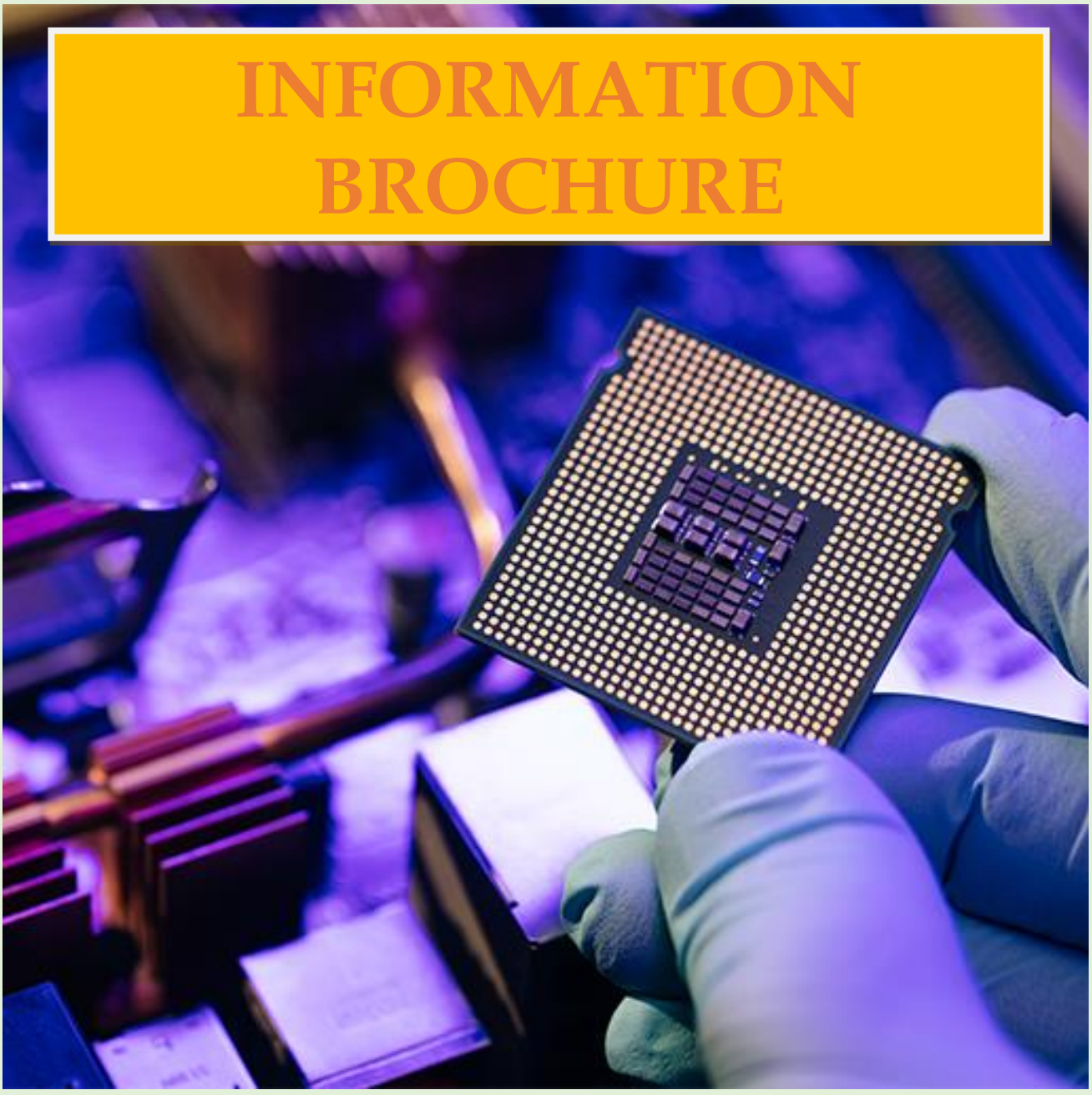
# NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

# INFORMATION BROCHURE



# National Institute of Electronics and Information Technology, NOIDA

**Name of Group:** Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

**Name of Course:** One-week Short Term Course & Training Program on VLSI Design

**Objective:** The one-week VLSI course aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with **Cadence EDA toolsuite**, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

**Duration:** 5 Days (40 Hours)

**NOTE:** Only in physical mode. **Limited seats (Only 20)**

**Eligibility:** Students who have completed or pursuing B.E. / B.Tech. / M.E / M.Tech.
**Note**: Research Scholars, Faculty members and Industry professionals can also enrol
**Prerequisites: -**

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

**Course Fees:** Rs. 3,540/- (incl. GST)

**Course Date:** 26 December 2023 to 30 December 2023

**Registration Process:** Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/ or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees Rs. 3,540/- (incl. GST) has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

**Course Content:**

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| **Day 1** | |
| 1st Half | **Inauguration & Invited talk** |
| 1st Half | **FPGAs:** Types, Architecture, Applications |
| 2nd Half | **FPGAs: Hands on Session**<br>1. HDL Design, Simulation<br>2. Dumping Code into FPGA<br>3. Hardware Debugging<br>4. Mark Debug Feature<br>5. Integrated Logic Analyzer (ILA) core |
| **Day 2** | |

**Partha P. Adhikari**,
Additional Director/Scientist 'E'
& OIC, CoE Chip Design Noida Centre

**PRASHANT PAL**
**(Scientist-C)**

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| 1st Half | **Synthesizing RTL Design on FPGA: Lecture, Demonstration, Lab session** |
| 2nd Half | **Hands on Session**<br>1. FPGA based Synthesis, Design and Implementation<br>2. Implementation and Static Timing Analysis |
| **Day 3** | |
| 1st Half | **ASIC Design Flow: Lecture, Demonstration, Lab session**<br>1. Semi-custom Design Flow<br>2. Full-custom Design Flow<br>3. IP Development |
| 2nd Half | **RTL Design & Verification: Lecture, Demonstration, Lab session**<br>1. Overview of RTL Integration<br>2. RTL Linting Concepts<br>3. Clock Domain Crossing Concepts<br>4. SoC Methodology & IP Integration<br>5. System Verilog<br>6. UVM, OVM, System C<br>7. Verification IPs |
| **Day 4** | |
| 1st Half | **Synthesis: Lecture, Demonstration, Lab Session**<br>1. Compilation<br>2. Elaboration<br>3. Various Synthesis Optimization Techniques<br>4. Low Power Features (IEEE 1801-2018)<br>5. Physical Aware Synthesis Flow<br>6. Optimization wrt Area & Timing Concepts<br>7. Synthesis Output: Netlist, Abstract Models, Hard Macros etc.<br>8. Unified Power Format (UPF), Logical equivalence Check Concepts |
| 2nd Half | **DFT (Design for Testability): Lecture, Demonstration, Lab Session**<br>1. Basics of DFT<br>2. Test Architecture<br>3. Scan Chain Insertion, Compression Insertion<br>4. Clock & Reset Controllability<br>5. ATPG<br>6. JTAG, Boundry Scan<br>7. MBIST/LBIST |
| **Day 5** | |
| 1st Half | **DFT Lab Session Contd….** |
| 2nd Half | **Physical Design: Lecture, Demonstration, Lab Session**<br>1. Floorplan, Placement, Routing<br>2. CTS<br>3. Multiple Clocks and Exceptions |
| 2nd Half | **Q & A** |

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* There will be 8 Hours Session per day.

**Mode of Payment:** Fees can be paid either by debit/credit card or in any online mode.
For any queries and more details please contact on **8218724641/9711177638**

**Course Venue**

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

**Registration Link:**
https://regn.nielitvte.edu.in/
or
Through Android App "**NIELIT Kaushal Setu**"

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