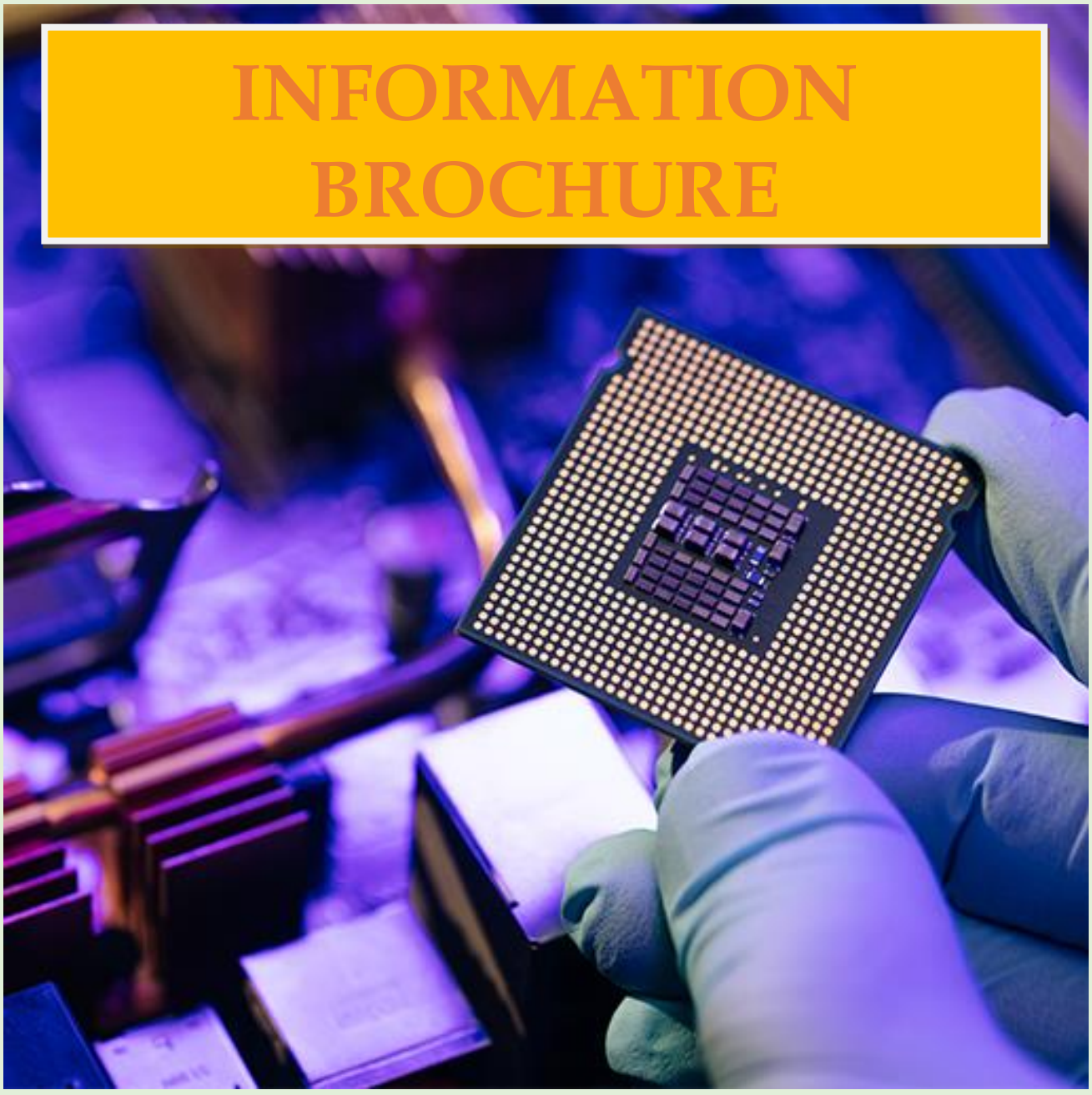
NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

INFORMATION BROCHURE



National Institute of Electronics and Information Technology, NOIDA

Name of Group: Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoC Teamup Semiconductors Pvt Ltd as industry partner

Name of Course: 5Day Short Term Course & Training Program on VLSI Design

Objective: The one-week VLSI course aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with **Cadence EDA toolsuite ,** explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Duration: 5 Days (30 Hours)

NOTE: Only in physical mode. **Limited seats (Only 20)**

Eligibility: Students who have completed or pursuing B.E. / B.Tech. / M.E / M.Tech.
Note: Research Scholars, Faculty members and Industry professionals can also enrol
Prerequisites: -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

Course Fees: Rs. 2,950/- (incl. GST)

Course Date: 21 August 2024 (Tentative)

Registration Process: Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees Rs. 3,540/- (incl. GST) has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

Course Content:

Day 1	**Inauguration & Invited talk**
	Full custom IC design flow
	Hands on Session with Cadence Virtuoso Tool • Schematic Creation Using Virtuoso Schematic Editor • Symbol Creation Using Virtuoso Symbol Editor • Layout Creation Using Virtuoso Layout Editor
Day 2	**Linux and VI Editor** • RTL Design Using HDL

PRASHANT PAL
(Scientist-C)

	• Introduction to Verilog syntax and constructs • Designing combinational and sequential logic using HDL • Writing RTL code for basic digital circuits **Hands on Training-** • **Code a design** • **Compile** • **Elaborate** • **Simulate design using Cadence xcelium**
Day 3	Basic Synthesis Flow -Input required for synthesis, synthesis stages, optimization techniques for best area , power and timing **Hands on training on** • Synthesizing RTL designs for target technologies , Elaboration • Optimizing design for area, power, and performance report generation
Day 4	**Physical Design** Perform basic physical design tasks which include • Floor planning • Clock tree synthesis • Placement • Power planning • Routing and constraint management • GDS generation. • Static timing analysis
	Hands on Training session: • **Run placement** • **Optimization** • **Clock tree synthesis** • **Routing on your design**
Day 5	• Static Timing Analysis

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	• Gate level Simulation • Run signoff checks to make sure that the design chip can be fabricated. • Write out a GDSII • Quiz

* There will be 6 Hours Session per day.

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode.
For any queries and more details please contact on **8218724641/9711177638**

Course Venue

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:

https://regn.nielitvte.edu.in/m/m-courseinfo.php?ci=178

or

Through Android App "**NIELIT Kaushal Setu**"

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