

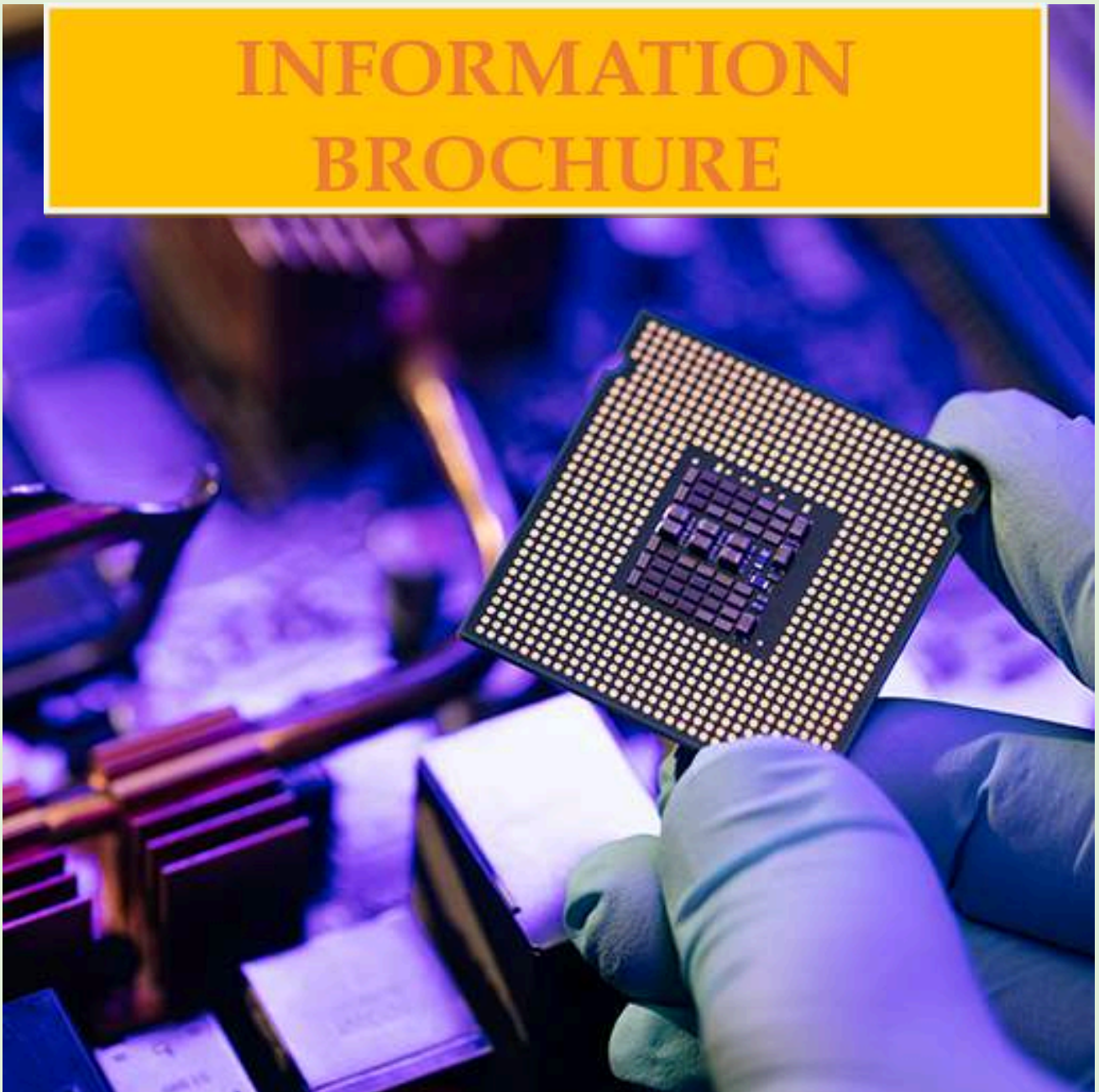


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# NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

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## INFORMATION BROCHURE



**Name of Group:** Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

**Name of Course:** One-week Short Term Course & Training Program on VLSI Design

**Objective:** The one-week VLSI course aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with **Cadence EDA tool suite**, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

**Duration:** 5 Days (30 Hours)

**NOTE:** Only in physical mode. **Limited seats (Only 20)**

**Eligibility:** Students who have completed or pursuing B.E. / B.Tech. / M.E / M.Tech.

**Note:** Research Scholars, Faculty members and Industry professionals can also enrol

**Prerequisites:** -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

**Course Fees:** Rs. 2,950/- (incl. GST)

**Course Date:** 18th March 2024 (Tentative)

**Registration Process:** Candidates have to apply in prescribed application form through online registration portal <https://regn.nielitvte.edu.in> or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees Rs. 3,540/- (incl. GST) has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

**Course Content:**

Day 1	<b>Inauguration &amp; Invited talk</b>
	<b>FPGAs:</b> Types, Architecture, Applications
	<b>FPGAs: Hands on Session</b> <ol style="list-style-type: none"><li>1. HDL Design, Simulation</li><li>2. Dumping Code into FPGA</li><li>3. Hardware Debugging</li><li>4. Mark Debug Feature</li><li>5. Integrated Logic Analyzer (ILA) core</li></ol>

**Partha P. Adhikari**  
Additional Director/Scientist 'E'  
& OIC, CoE Chip Design Noida Centre

**PRASHANT PAL**  
(Scientist-C)

<b>Day 2</b>	<b>Synthesizing RTL Design on FPGA: Lecture, Demonstration, Lab session</b>
	<b>Hands on Session</b> 1. FPGA based Synthesis, Design and Implementation 2. Implementation and Static Timing Analysis
<b>Day 3</b>	<b>ASIC Design Flow: Lecture, Demonstration, Lab session</b> 1. Semi-custom Design Flow 2. Full-custom Design Flow 3. IP Development
	<b>RTL Design &amp; Verification: Lecture, Demonstration, Lab session</b> 1. Overview of RTL Integration 2. RTL Linting Concepts 3. Clock Domain Crossing Concepts 4. SoC Methodology & IP Integration 5. System Verilog 6. UVM, OVM, System C 7. Verification IPs
<b>Day 4</b>	<b>Synthesis: Lecture, Demonstration, Lab Session</b> 1. Compilation 2. Elaboration 3. Various Synthesis Optimization Techniques 4. Low Power Features (IEEE 1801-2018) 5. Physical Aware Synthesis Flow 6. Optimization wrt Area & Timing Concepts 7. Synthesis Output: Netlist, Abstract Models, Hard Macros etc. 8. Unified Power Format (UPF), Logical equivalence Check Concepts
	<b>DFT (Design for Testability): Lecture, Demonstration, Lab Session</b> 1. Basics of DFT 2. Test Architecture 3. Scan Chain Insertion, Compression Insertion 4. Clock & Reset Controllability 5. ATPG 6. JTAG, Boundry Scan 7. MBIST/LBIST
<b>Day 5</b>	<b>DFT Lab Session Contd....</b>
	<b>Physical Design: Lecture, Demonstration, Lab Session</b> 1. Floorplan, Placement, Routing 2. CTS 3. Multiple Clocks and Exceptions
	<b>Q &amp; A</b>

\* There will be 6 Hours Session per day.

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# National Institute of Electronics and Information Technology, NOIDA

**Mode of Payment:** Fees can be paid either by debit/credit card or in any online mode.  
For any queries and more details please contact on **8218724641/9711177638**

## **Course Venue**

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahmampurtra Shopping  
Complex Sector 29, Noida, Uttar Pradesh 201301

## **Registration Link:**

<https://reg.nielitvte.edu.in/m/m-courseinfo.php?ci=178>

or

Through Android App "[NIELIT Kaushal Setu](#)"

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